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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Robert J. Custer

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EXAMINER

THOMAS, LUCY M

ART UNIT

PAPER NUMBER

2836

DATE MAILED: 09/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,257	CUSTER ET AL.	
	Examiner	Art Unit	
	Lucy Thomas	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 June 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5,7-21 and 24-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5,7-21,24-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-5, 8-10, 13-21, and 24-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gohlke (US 2004/0061379) in view of Gerlach (US 2002/0054465).

Regarding Claim 1, Gohlke discloses an electrical transient protection circuit in a vehicle (Figures 6A-C), comprising: an input connector 101 receiving an input voltage; means for absorbing 102 electrically connected to the input connector; means for blocking 103, 104 electrically connected to the input connector, and at least one of the means for absorbing and means for blocking conditioning the input voltage by suppressing a voltage transient and producing a corresponding output voltage, and an output connector (coupled to output 105 in Figure 6C) delivering the output voltage, to an electrical component of the vehicle (Paragraphs 39, 40, 42, 47, 50, 53).

Gohlke does not disclose the means for absorbing including a plurality of metal oxide varistors having different voltage ratings. Gerlach discloses a surge protector (see Figure 1) wherein the means for absorbing includes plurality of metal oxide varistors 41, 42 having different voltage ratings (Paragraphs 4, 43). It would have been obvious to those skilled in the art at the time the invention was made to modify Gohlke's circuit with a plurality of metal oxide varistor with different voltage ratings as taught by

Art Unit: 2836

Gerlach, because metal oxide varistors provide surge transient protection for many low voltage applications, with nominal operating voltages of about six hundred volts or less (Gerlach, Paragraph 4).

The voltage transients being up to i) about 8 times the input voltage through a source impedance of about 0.4 ohm for about 0.5 seconds, ii) about 50 times the input voltage through a source impedance of about 20.0 ohm for about 1.0 millisecond, and iii) about 50 times a negative of the input voltage through a source impedance of about 20.0 ohm for about 1.0 millisecond, and that the output voltage is less than and equal to about 10% above the input voltage is disclosed by Gohlke in the table in Paragraph 50. Standard acceptable levels for voltage transients are disclosed by the American National Standards for load dump and inductive switching in vehicles and can be found in industry documents (Page 36, Table 4A, Table 4B, SAE J1455). With regard to the voltage transient, it can be recognized from the established standards that the range of the voltage transient would fall into the ranges specified by the standards. It is understood that the output voltage would be about 10% above the input voltage to accommodate the tolerances associated with the circuit components so that the output voltage is less than about 110% of the input voltage.

Regarding Claim 2, Gohlke discloses the electrical transient protection circuit, wherein the means for blocking includes a field effect transistor 112 (see Figure 6C, Paragraph 42).

Regarding Claim 3, Gohlke in view of Gerlach discloses the electrical transient protection circuit, wherein the means for absorbing absorbs a first portion of the voltage

transient and the means for blocking blocks a second portion of the voltage transient; and the second portion may represent up to all of the voltage transient (Paragraphs 5, 6).

Regarding Claim 4, Gohlke discloses an n-channel switching field effect transistor 143 (Paragraph 45). Regarding Claim 5, Gohlke discloses a p-channel switching field effect transistor 112 or 114 (see Figure 6B).

Regarding Claim 8, Gohlke discloses the electrical transient protection circuit, wherein the means for blocking controls an electrical connection between the input connector and the output connector as a function of the voltage transient (see Abstract, Paragraphs 5 and 39). Regarding Claim 9, Gohlke discloses the electrical transient protection circuit, wherein the means for absorbing and means for blocking operate independently of each other (Paragraphs 36 and 37).

Claim 10 differs from Claim 1 in that Claim 10 is limited only as an over voltage transient protection circuit instead of an electrical transient protection circuit as Claim 1, and the output voltage is limited to less than about 200%, instead of 110% as in Claim 1, of the input voltage. Since Claim 10 recites the broader limitation, it may also be rejected on the same basis as Claim 1.

Regarding Claim 13, Gohlke discloses that the means for blocking includes an n-channel field effect transistor 127.

Regarding Claim 14, Gerlach does not disclose that one of the metal oxide varistors is rated up to about 150 volts. It would have been obvious to those skilled in the art at the time the invention was made to select the rating of the varistor based on

Art Unit: 2836

the expected voltages that are going to occur in the circuit and the desired cutoff level of the voltage transients spikes. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Regarding Claim 15, Gohlke discloses the over voltage transient protection circuit, wherein the means for absorption absorbs a first portion of the voltage transient and the field effect transistor (means for blocking) blocks a second portion of the voltage transient, and the second portion may represent up to all of the voltage transient (Paragraph 6).

Claim 16 basically recites elements of Claims 1. Therefore, please refer to the above rejection of Claim 1. Claim 17 recites the elements of Claim 9. Therefore, please see the rejection for Claim 9.

Claim 18 recites the elements of Claim 2 with the additional limitation of 150 volts rating for the MOV as recited in Claim 14 and 150 volts rating for a first FET. Gohlke does not disclose that the FET is rated about 150 volts. It would have been obvious to those skilled in the art at the time the invention was made to select the rating of the transistors based on the expected voltages that are going to occur in the circuit and the desired cutoff level of the voltage transients spikes. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Regarding Claim 19, Gohlke discloses that the means for blocking which includes a second field effect transistor 114, a state of the second field effect transistor being controlled as a function of the first field effect transistor.

Claim 20 basically recites elements of Claim 15. Therefore, please see the rejection of Claim 15. Regarding Claim 23, Gohlke discloses the means for absorbing which includes a transient voltage suppressor 107, or, 109, or 111 (Paragraph 40).

Claims 21, and 24 basically recite an electrical transient protection circuit with elements disclosed in Claims 16 and part of Claim 18, except that the means for absorbing and means for blocking recited in Claims 16 and 18 are recited as electronic components, which are taught by the prior art references. Therefore, please refer to the above rejection.

Regarding Claims 25-27 and 29, the recited method steps would necessarily be performed when implementing the electrical transient protection circuit recited in Claims 1 and 10. For example, regarding Claim 26, Gohlke discloses said absorbing which includes absorbing the second portion of the voltage transient having about 600 Volts said blocking which includes the first portion of the voltage transient having about 150 Volts (Paragraph 6). The recited about 600 Volts is the transient voltage as set by the industry standard, and 150 Volts is the resultant of voltage division across the source impedance and the blocking means.

Regarding Claim 28, Gohlke discloses the method for suppressing electrical transients, wherein the blocking includes setting a field effect transistor 112 or 114 to an open state (Paragraph 44, lines 28-31, Paragraph 53).

Art Unit: 2836

3. Claims 7, and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gohlke (US 2004/0061379) in view of Gerlach (US 2002/0054465) and Allman (US 5,410,441). Regarding Claim 7, Gohlke discloses the electrical transient protection circuit further including a field effect transistor Q28. Gohlke does not disclose a body diode electrically oriented for blocking a negative of the input voltage. Allman discloses an electrical transient protection circuit (Figure 1) including a field effect transistor 101 having a body diode electrically oriented for blocking a negative of the input voltage (Column 2, lines 41-46). It would have been obvious to those skilled in the art at the time the invention was made to modify Gohlke's circuit with a field effect transistor having a body diode as taught by Allman, because the body diode which is reverse biased when the input voltage is negative and is effective as a block against current flow through the load.

Regarding Claim 11, Allman discloses the over voltage transient protection circuit (Figure 1), wherein the means for absorbing includes a first field effect transistor 101 having a drain electrically connected to the input voltage, and further including a second FET 102 having a source connected to the source of the first transistor and gate electrically connected to the gate of the first transistor, a state of the first transistor being controlled as a function of the input voltage, and state of the second transistor being controlled as a function of a state of the first transistor, the second FET providing the protection against a negative input voltage (Column 2, lines 28-45).

Regarding Claim 12, Gohlke and Allman do not disclose that the first FET is rated about 150 volts and the second FET is rated up to about 150 volts. It would have

Art Unit: 2836

been obvious to those skilled in the art at the time the invention was made to select the rating of the transistors based on the expected voltages that are going to occur in the circuit and the desired cutoff level of the voltage transients spikes. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.

In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Response to Arguments

4. Applicant's arguments filed 6/27/2006 have been fully considered.

Gerlach discloses a surge protector (see Figure 1) wherein the means for absorbing includes plurality of metal oxide varistors 41, 42 having different voltage ratings (Paragraphs 4, 43), and the reference is relied upon to show the teaching of plurality of metal oxide varistors (metal oxide varistors provide surge transient protection for many low voltage applications, with nominal operating voltages of about six hundred volts or less (Gerlach, Paragraph 4)). Therefore, the references, Golke and Gerlach combined, meet the limitations of the amended Independent Claims 1, 10, 16, 21, and 25.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2836

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lucy Thomas whose telephone number is 571-272-6002. The examiner can normally be reached on Monday - Friday 8:00 AM - 4:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2836

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LT
September 06, 2006



BURTON S. MULLINS
PRIMARY EXAMINER